IN THE CLAIMS:

Please cancel claim 11. **Please also amend** claims 1-10, 12-22, and 24-31 as shown in the complete list of claims that is presented below.

1. (currently amended) A method for accessing initialization data for starting a central processor unit in a computer system comprising:

(a) starting up a north-bridge chip that is connected between the central processor unit and a bus;

(b) sending a request for ~~requesting~~ said initialization data ~~by~~ from said north-bridge chip ~~from~~ to a south-bridge chip that is connected to the bus and;

(c) receiving said initialization data by said north-bridge ~~chip.~~ chip.

2. (currently amended) The method according to Claim 1 wherein said initialization data is serial initialization packet ("SIP") ~~[?]~~ data of the central processor unit.

3. (currently amended) The method according to Claim 2 wherein said initialization data is SIP data ~~of~~ for an AMD K7 processor.

4. (currently amended) The method according to Claim 1 wherein ~~the starting up a north-bridge chip further includes~~ step (a) comprises starting up the north-bridge chip by said south-bridge chip.

5. (currently amended) The method according to Claim 1 wherein ~~the requesting further includes~~ step (b) comprises sending a signal from said north-bridge chip to said south-bridge chip for requesting said initialization data.

6. (currently amended) The method according to Claim 1 further comprising sending said initialization data from said north-bridge chip to the central processor unit of said computer system for starting up the central processor unit.

7. (currently amended) A method for accessing initialization data ~~of~~ for a central processor unit by a south-bridge chip connected to a bus in a computer system that also includes a north-bridge chip connected between the bus and the central processor unit, said method comprising:

(a) accessing said initialization data by said south-bridge chip; and

(b) sending said initialization data ~~by~~ from said south-bridge chip to said north-bridge chip and thence to said central processor unit.

8. (currently amended) The method according to Claim 7 wherein said initialization data is SIP data ~~of~~ for an AMD K7 processor.

9. (currently amended) The method according to Claim 7 wherein said south-bridge chip accesses said initialization data during step (a) from a boot ROM of said computer system.

10. (currently amended) The method according to Claim 7 ~~wherein~~ further comprising using said south-bridge chip ~~accesses said initialization data after a~~ to start up said north-bridge chip ~~of said computer system is started up by said south-bridge chip and sends a signal to request said initialization data~~ before step (a) is conducted.

Claim 11 (cancelled).

12. (currently amended) A method for accessing initialization data for starting a central processor unit in a computer system that also includes a bus, a south-bridge chip connected to the bus, a non-volatile memory that stores the initialization data, and a north-bridge chip connected between the bus and the central processor unit, the method comprising:

(a) ~~requesting~~ sending a request for the initialization data ~~by a~~ from the north-bridge chip ~~from a~~ to the south-bridge chip;

(b) ~~accessing the initialization data stored in a non-volatile memory by~~ using the south-bridge chip to access the non-volatile memory and read out the initialization data; ~~and~~

(c) sending the initialization data from the south-bridge chip to the north-bridge chip; and

(d) activating the central processor unit based on the initialization data received by the north-bridge chip from the south-bridge chip.

13. (currently amended) The method of claim 12 further comprising activating the north-bridge chip by sending an initiating signal from the south-bridge chip before step (a) is conducted.

14. (currently amended) The method of claim ~~1-2further~~ 13, further comprising activating the south-bridge chip by a power supplier before sending an initiating signal from the south-bridge chip to actuate the north-bridge chip.

15. (currently amended) The method of claim 12 wherein the non-volatile memory is a read only memory containing a BIOS.

16. (currently amended) The method of claim ~~1-2~~ 12 wherein the ~~requesting further includes sending~~ request sent in step (a) is a transaction sent from the north-bridge chip to the south-bridge chip requesting the south-bridge chip to retrieve the initialization data from the non-volatile memory.

17. (currently amended) The method of claim 12 wherein ~~the activating further~~ step (d) includes:

receiving the initialization data by the north-bridge chip; and

sending an initializing signal and the received initialization data to the central processor ~~unit.~~ unit.

18. (currently amended) The method of claim 17 wherein the initialization data ~~further~~ includes an initialization ID.

19. (currently amended) The method of claim 17 wherein the initialization data ~~further~~ includes serial initialization packet ("SIP") data.

20. (currently amended) A system for accessing initialization data for starting a central processor unit, the system comprising:

a south-bridge chip;

a north-bridge chip in direct communication with ~~a~~ the south-bridge chip and the central processor unit; and

a non-volatile memory subsystem in direct communication with the south-bridge chip storing the initialization data;

wherein upon receiving a request from the north-bridge chip for obtaining the initialization data, the initialization data is accessed by the south-bridge chip and forwarded to the north-bridge chip for activating the central processor unit.

21. (currently amended) The system of claim 20 further comprising a power supplier for activating the south-bridge chip.

22. (currently amended) The system of claim 20 wherein the non-volatile memory is a read only memory containing a BIOS.

23. (original) The system of claim 22 wherein the non-volatile memory includes a predetermined location for storing the initialization data that is not occupied by the BIOS.

24. (currently amended) The system of claim 20 wherein the initialization data ~~further~~ includes an initialization ID.

25. (currently amended) The system of claim 20 wherein the initialization data ~~further~~ includes session initialization protocol data.

26. (currently amended) The system of claim 20 wherein the south-bridge chip ~~further~~ includes means for:

activating the north-bridge chip;

retrieving the initialization data by the south-bridge chip; and

sending the initialization data to the north-bridge chip.

27. (currently amended) The system of claim 20 where in the north-bridge chip further includes means for sending an initializing signal to the central processor unit based on the forwarded initialization data.

28. (currently amended) A method for accessing initialization data for starting a central processor unit in a computer system, the method comprising:

activating a south-bridge chip by a power supplier controller;

activating a north-bridge chip by the activated south bridge chip;

requesting the south-bridge chip to access the initialization data, the initialization data being stored in a non-volatile memory;

accessing the initialization data stored in ~~a~~ the non-volatile memory by the south-bridge chip;

sending the initialization data to the north-bridge chip ~~by~~ from the south-bridge chip;

sending an initialization signal to the central processor unit ~~by~~ from the north bridge chip upon receiving the initialization data; and

activating the central processor unit ~~by~~ using the initialization signal.

29. (currently amended) The method of claim 28 wherein the non-volatile memory is a read only memory containing a BIOS.

30. (currently amended) The method of claim 28 wherein the initialization data ~~further~~ includes an initialization ID.

31. (currently amended) The method of claim 28 wherein the initialization data ~~further~~ includes session initialization protocol data.